THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 32

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

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Ex parte STEPHEN E. BELLO,
KIEN A. HUA, and
JIH-KWON PEIR

_____

Appeal No. 96-3236
Application 08/295,493[1]

_____

ON BRIEF

_____

Before THOMAS, KRASS and CARMICHAEL, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 8, 10 through 13, 15 through 21, 23, 24, 26, 27, 29 through 54, 56, 57, 59 and 60, all of the claims remaining in the

[1] Application for patent filed August 25, 1994. According to appellants, this application is a continuation of Application 07/845,973, filed March 4, 1992.

application.

The invention pertains to an error detection scheme for a multiple processor system which uses compressed signature collection and voting techniques to ensure process integrity.

Representative independent claim 1 is reproduced as follows:

1. A multiprocessor computer system with error detection capability for processing multiple instruction sets, each instruction set of said multiple instruction sets comprising a plurality of instructions, said multiprocessor computer system comprising:

a plurality of processors, each processor independently and asynchronously processing at least some of said multiple instruction sets from the other of said plurality of processors;

a plurality of hardware signature generation means, each hardware signature generation means being associated with a respective processor of said plurality of processors for generating a compressed hardware signature contemporaneous with and substantially uniquely corresponding to said respective processor's processing of a selected instruction set of said multiple instruction sets;

selection means for identifying said selected instruction set for comparison of respective compressed hardware signatures from at least two hardware signature generation means of said plurality of hardware signature generation means; and

voting means coupled to receive each of said respective compressed hardware signatures for comparing said signatures for an error condition, an error condition being identified if a predefined comparison failure is detected between the received compressed hardware signatures.

The examiner relies on the following references:

Danielsen et al. (Danielsen)	5,136,704	Aug. 4, 1992

		(Filed June 28, 1989)
Westcott et al. (Westcott)	5,151,981	Sept. 29, 1992
		(Filed July 13, 1990)

Claims 1 through 8, 10 through 13, 15 through 21, 23, 24, 26, 27, 29 through 54, 56, 57, 59 and 60 stand rejected under 35 U.S.C. § 103 as unpatentable over Danielsen in view of Westcott.

Reference is made to the briefs and answer for the respective positions of appellants and the examiner.

OPINION

We reverse.

Each and every one of independent claims 1, 17, 26, 37, 50, 59 and 60 requires processors operating "asynchronously." The primary reference to Danielsen, while directed to error detection in multiprocessor systems, makes it very clear that the processors therein are run synchronously. Column 5, lines 52-55 of Danielsen indicates that processor A, its key generator 48 and its lock circuit 50 are all started "and run in synchronism with each other and with processor B, its key generator 62, and its lock circuit 64." Even in the situation where two clocks are employed in the system rather than one

clock running all operations, Danielsen states (column 7, lines 67-68) that the "two clocks would need to be synchronized with each other."

Thus, it is clear that while the claims require processors operating asynchronously, the primary reference employed by the examiner to reject those claims discloses a system which operates only in a synchronous manner. The examiner does not deny this.

Rather, the examiner states, that it would have been obvious "to modify Danielsen to independently clock Danielsen's processors because one would want to prevent catastrophic failure of Danielsen's Anti-Lock Brakes if said one clock fail [sic]" [answer-page 4]. The examiner further states that it would have been obvious "to modify Danielsen to asynchronously (loosely-coupled) operate his processors because this would add greater reliability to his system" [answer-page 5].

The examiner's rationale, in our view, is based on impermissible hindsight gleaned from appellants' own disclosure. At page 2 of the specification, appellants disclose that a drawback to the TMR (triple module redundancy) system is that because the modules share a common clock, "clock failure is devastating to operation of the system." They also disclose that while "loose synchronization" between processors is known when using a software data collection and voting technique, the

drawback to such systems is the "extensive communications overhead required" [pages 2-3 of the specification]. It appears to us that appellants are the ones who have recognized the drawbacks to the various prior art techniques and the manner of improving such techniques. Thus, it appears that the examiner uses the rationale (e.g., catastrophic consequences if the clock in a single clock system fails) referred to by appellants as a reason for operating processors asynchronously and concludes that it would have been obvious to do what appellants have done for the reasons appellants did it. 35 U.S.C. § 103 requires more. There must be some suggestion in the prior art, or some convincing rationale as to the level of artisans which would have led them, to do what appellants have done.

Additionally, without a specific direction to do so, there would appear to be no reason to change a synchronous operation to an asynchronous one. The examiner has not shown any suggestion in the prior art for modifying Danielsen's system to make it asynchronous in the face of Danielsen's explicit disclosure of a synchronous system. Nor has the examiner shown us, by convincing evidence, that the skilled artisan would have been led, for any reason other than that given by appellants, to have provided for asynchronous operations of the processors in Danielsen.

Westcott is of no help in providing for the deficiency of Danielsen, Westcott being applied by the examiner merely as a teaching of a selection means to select a particular instruction from a group of instructions.

We need not address the issues of whether the applied references teach or suggest the claimed "compressed hardware signature..." or the "selection means" as it relates to the compressed hardware signatures since, in our view, the examiner has not even gotten past the "asynchronously processing" requirement of the claims.

Accordingly, the examiner's rejection of claims 1 through 8, 10 through 13, 15 through 21, 23, 24, 26, 27, 29 through 54, 56, 57, 59 and 60 under 35 U.S.C. § 103 is reversed.

REVERSED

JAMES D. THOMAS	)
Administrative Patent Judge	)
	)
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	) BOARD OF PATENT
ERROL A. KRASS	)
Administrative Patent Judge	) APPEALS AND
	)
	) INTERFERENCES
	)
JAMES T. CARMICHAEL	)
Administrative Patent Judge	)

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